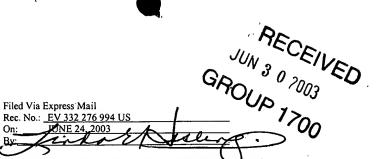


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Any fee due as a result of this paper, not covered by an endlosed check, may be charged on Deposit Acct. No. 50-1290.

Attorney Docket No.: NECW 18.159

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#10A 7/1/03

Inventor

: Atsushi NISHIZAWA

Serial No.

: 09/751,979

Filed

: December 29, 2000

Title

: MANUFACTURING METHOD OF SEMICONDUCTOR

INTEGRATED CIRCUIT INCLUDING SIMULTANEOUS

FORMATION OF VIA HOLE REACHING METAL WIRING AND CONCAVE GROOVE IN INTERLAYER FILM AND SEMICONDUCTOR INTEGRATED CIRCUIT MANUFACTURED WITH THE MANUFACTURING METHOD

Examiner

: George A. Goudreau

Group Art Unit

: 1763

Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

AMENDMENT

SIR:

In response to the Office Action dated February 24, 2003, the period for response not being extended for more than one month, please amend the subject application as follows: